

# High Curvature Bending of Ultra-Thin Chips and Chip-on-Foil Assemblies

D.A. van den Ende<sup>1</sup> Jeroen van den Brand<sup>1</sup>

1. Holst Centre/TNO, High Tech Campus 31, 5656 AE Eindhoven, The Netherlands.

**Introduction:** Ultra-thin chips <20µm thick become flexible, allowing integration of silicon IC technology with highly flexible electronics [1,2].

Examples include:

- sensor systems in food packaging.
- monitoring tags for healthcare and sport in clothing or even as wearable patches directly on the skin.



Figure 1. Thin chip and skin sensor patch developed at Holst Centre

## Computational Methods:

- Linear elastic material model including geometric non-linearity
  - Large deformations are present in the structure
- Contact & sliding friction is encountered.
- Quasi static time dependency

$$-\nabla \sigma = F_V$$

$$s = s^0 + C : (\varepsilon - \alpha \theta \mathbf{I} - \varepsilon^0 - \varepsilon^i)$$

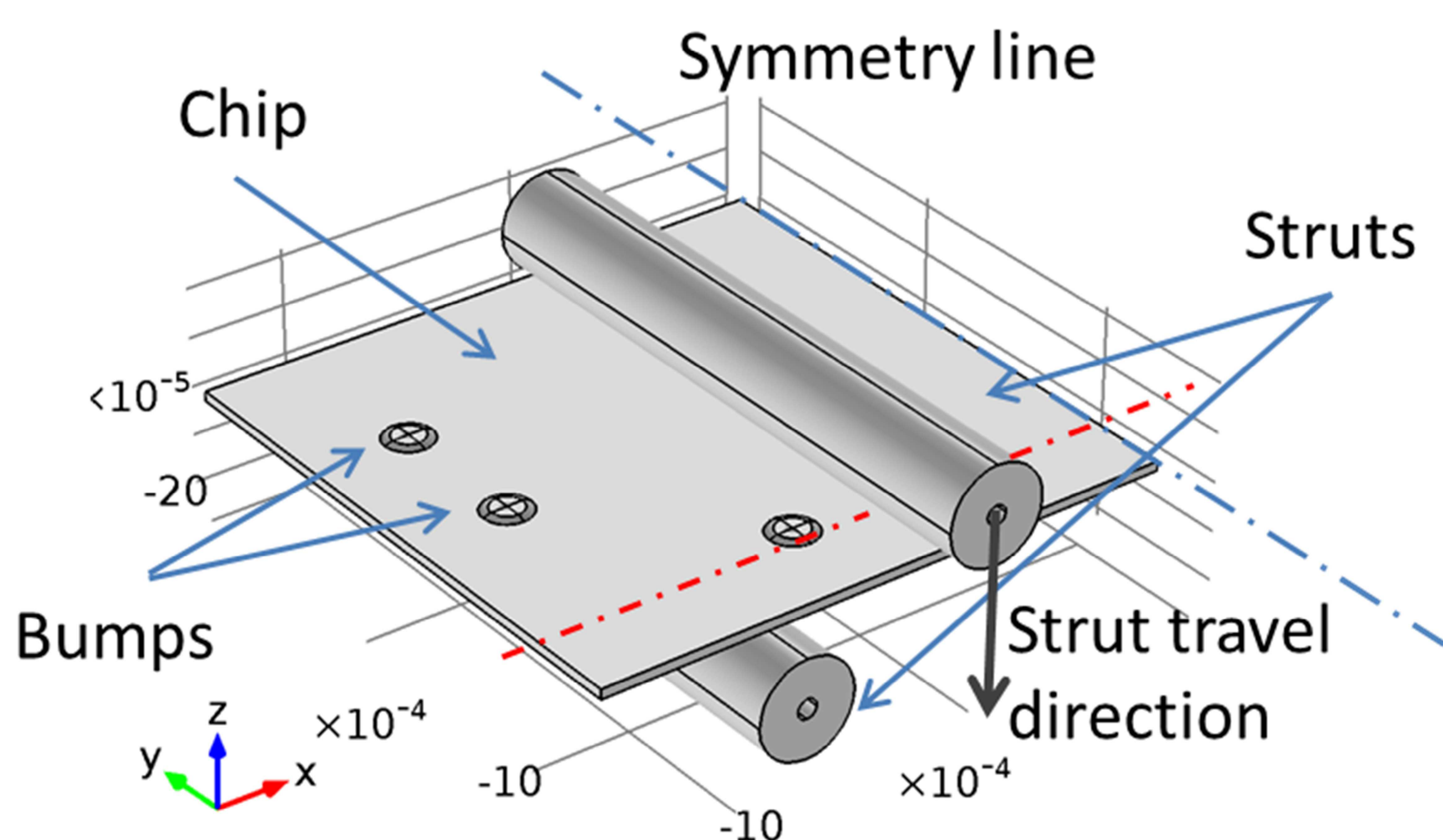


Figure 2. Four-point bending model of a thin chip.

**Results:** the stress distribution in xx-direction ( $S_{xx}$ ) in the bumped die is presented. The bottom of the die is subjected to tensile stress. The influence of the bumps is clearly visible at the bottom of the die.

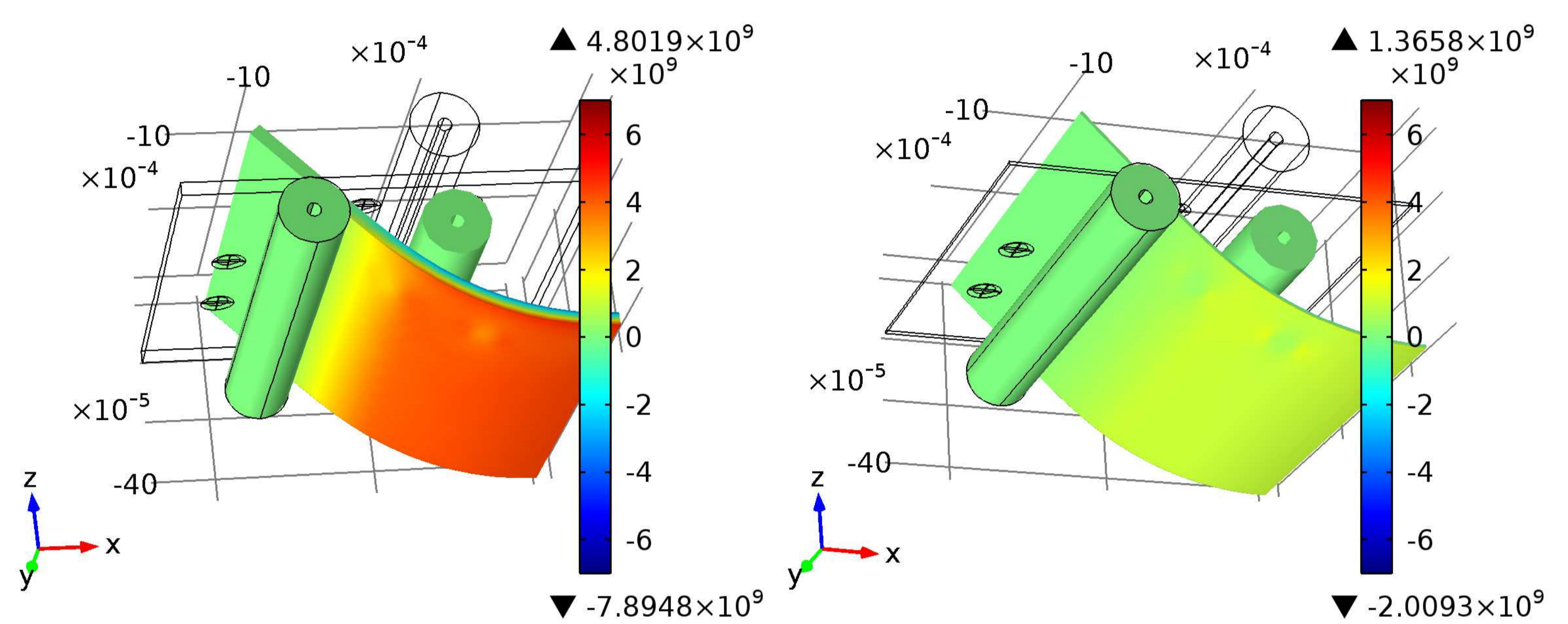


Figure 3. Stresses in chips with different thickness

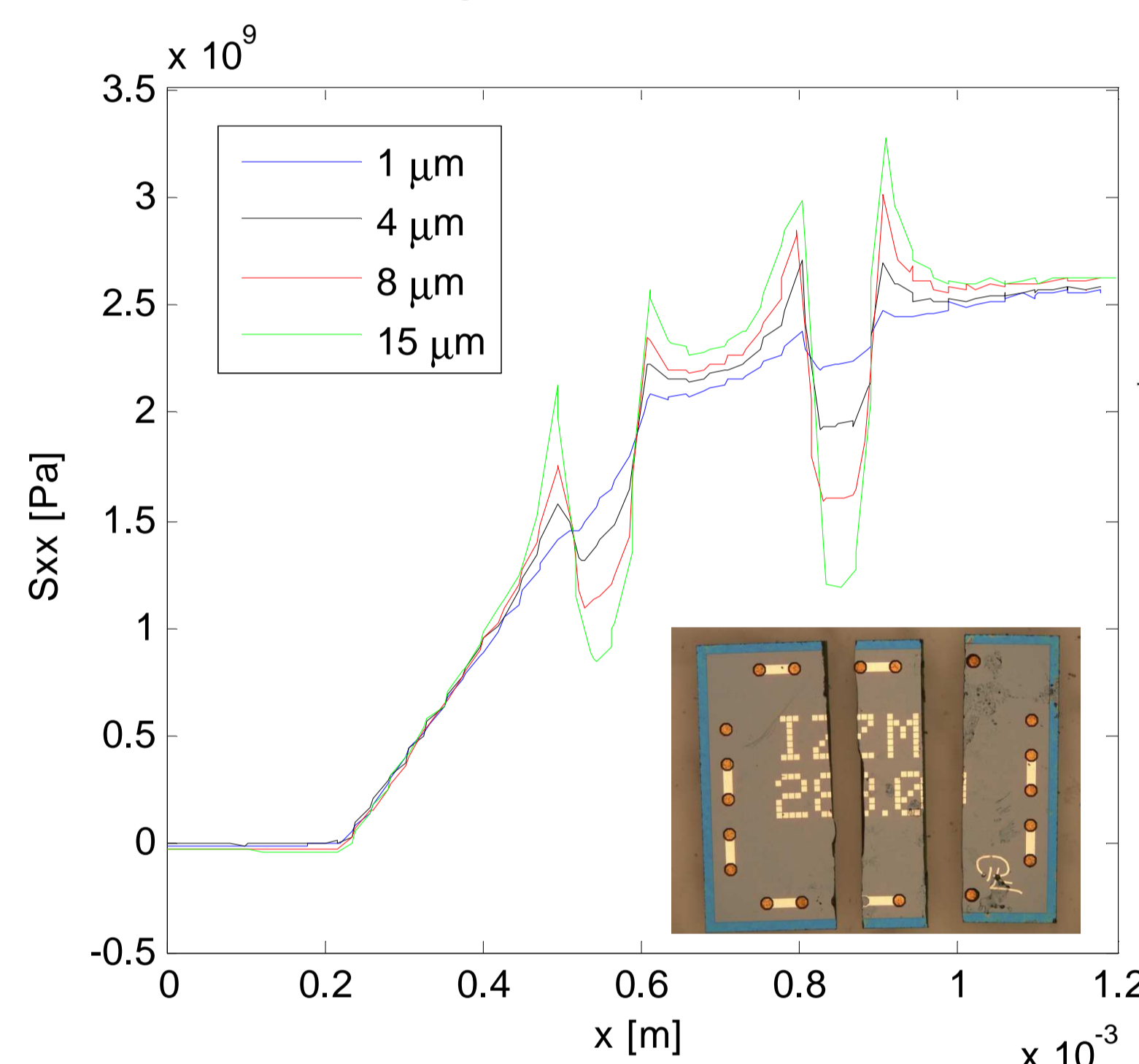


Figure 4. Stress concentrations at bump locations

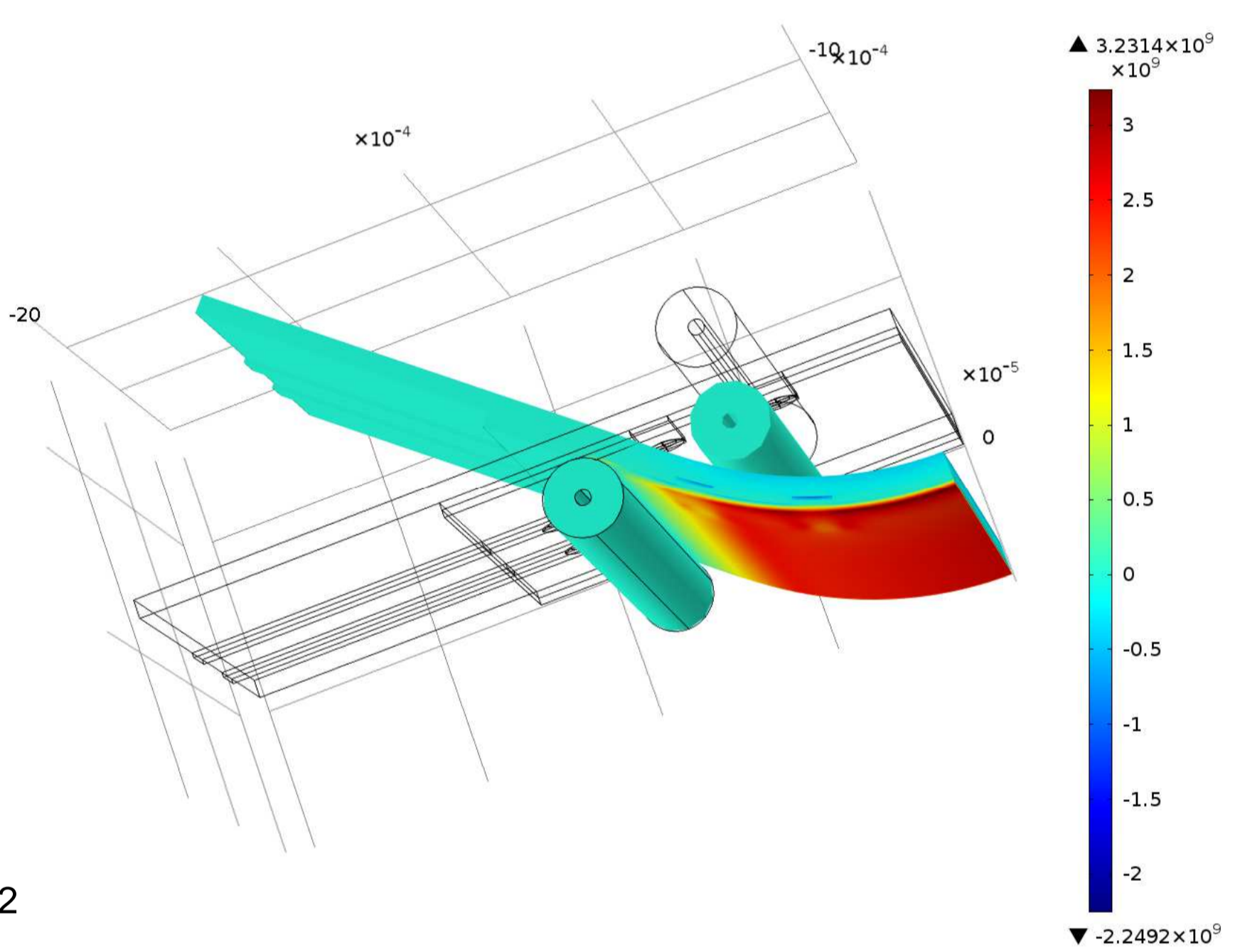


Figure 5. Chip-on-foil assembly at bump locations

## Conclusions:

- Chip failure locations correspond to stress concentrations in model
- Model can be used for optimizing chip on foil assemblies

## References:

1. J. Burghartz *et al.* *Solid-State Electronics* **54** 818–829 (2010)
2. J. van den Brand *et al.* "Proc. 18th European Microelectronics and Packaging Conference (EMPC), art. no. 614241 (2011)