Excerpt from the Proceedings of the 2011 COMSOL Conference in Boston

Power Transistor Heat Sink Design Trade-offs

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Abstract: Power transistors require heat sinks to dissipate thermal energy and keep junction temperatures below the recommended limit. The reliability and longevity of any semiconductor device is inversely proportional to the junction temperature. Hence, a significant increase in reliability and component life can be achieved by a small reduction in operating temperature. A range of heat sink designs and mounting procedures are available, each with reasonably predictable performance. However, it is possible to overdesign by incorporating a margin of safety that is too high. This paper describes the results obtained by modeling the heat transfer process in a TO-220 several heat sink configuration and discusses key design trade-offs.

The model was developed using COMSOL 4.2 and employs the heat transfer (ht) module for conduction in solids for use in stationary and parametric studies. The materials consisted of a plastic chip carrier, stainless steel mounting tab, copper conducting leads, and an aluminum heat sink. The model accounts for heat transfer due to radiation via emissivity and natural convection into ambient temperature air. Parametric studies were performed that considered heat sink size/area, emissivity and convective cooling coefficient to estimate the impact of each on steady-state temperature.

Keywords: power transistor, cooling, heat sink design, heat transfer.

1. Introduction

Heat sinks are commonly used in electronic circuits to help keep certain components from over-heating. Mostly, the focus of cooling centers on semiconductor devices where power consumption is often the greatest and high junction temperatures decreases the mean time to failure. A wide variety of heat sink configurations are available for designers to tailor an efficient and economical solution. In many cases, cooling fans are added to increase the convective cooling portion of the process.

This paper focuses on power transistor cooling and deals specifically with a TO-220 package, one of several common package types used in the industry. A 3-D COMSOL 4.2 model was developed to predict the temperature distributions within the transistor and heat sink for a range of power dissipation levels. Parametric studies were also performed to determine the impact of heat sink surface area, emissivity, and convective cooling (both natural and forced). The model development is similar to that reported by Comsol, Inc. for joule heating of a power transistor.[1]

2. Physical Geometry

The physical geometry of a TO-220 package is shown in Fig. 1. A single transistor die is housed within a plastic chip carrier (PLCC). Three leads (emitter, base and collector) are electrically connected to the die with wire bonds. The leads provide the external interface to the copper printed circuit traces. The collector of the transistor is mounted directly to a stainless steel case. The case provides a convenient path for heat conduction out of the transistor, but since it is connected to the collector, it must be electrically insulated from other metal components such as the heat sink body to prevent shorting. The case also has a mounting hole so it can be secured to the heat sink with a simple bolt/nut arrangement.

Figure 1. TO-220 transistor package.

Several alternatives are available to electrically insulate the case and heat sink. Our model was based on a thin 0.1mm sheet of mica. Even though mica is a poor heat conductor, the thickness of the slice can be made small yet still provide ample voltage protection. A thermal compound is typically applied to both sides of the mica sheet is eliminate small air pockets and improve heat conduction.

The physical geometry of the heat sink and transistor is shown in Fig. 2. It consists of a U-shaped body with 8 fins, 4 on each side, to increase surface area and air flow. The model includes a mounting bolt, but omits the nut and insulating washer to simplify the finite element mesh.

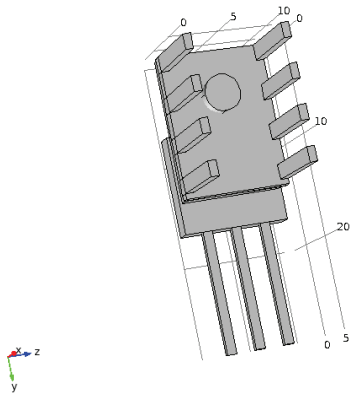

Figure 2. Heat sink mounted to transistor.

3. Material Composition and Properties

The TO-220 package and heat sink assembly consists of 7 different materials. The transistor die is made up completely of doped silicon while the 3 leads plus wire bonds are copper and gold, respectively. The transistor die, wire bonds and portions of the 3 leads are embedded in the PLCC. The case and mounting bolt are made from steel alloy AISI 4340 securing the aluminum alloy 6063 heat sink with a mica layer sandwiched between. Table 1 lists the materials and their assumed material properties for a generalized solution of the heat transfer process including time-dependent analysis (not performed in this study).

Table 1. Mechanical material properties.

Material	Density (kg/m^3)	Heat Capacity (J/kg-K)	Thermal Conductivity (W/m-K)
Silicon	2,300	710	150
Copper	8,700	385	400
Gold	19,300	129	318
PLCC	900	1,700	0.2
Steel AISI 4340	7,850	477	54
Mica	2,883	500	0.71
Aluminum Alloy 6063	2,700	900	200

The model accounts for surface-to-ambient radiation from the heat sink and TO-220 hence the emissivity for the appropriate materials is given in Table 2.

Table 2. Emissivity properties.

Material	Emissivity
Copper	0.85
PLCC	
Steel AISI 4340	
Black Anodized Aluminum Alloy 6063	0.77

4. Governing Equations

Heat conduction in solids is governed by Eq. 1 below.[2] For a steady state or stationary solution in time, the first term of Eq. 1 disappears, and the governing material property becomes thermal conductivity.

$$\rho C_p \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = Q \qquad (1$$

where ρ = density (kg/m^3)
C_p = heat capacity (J/kg-K)
k = thermal conductivity (W/m-K)
Q = heat source (W)
T = temperature (K)
t = time (s)

Four boundary conditions are employed within the model. First, convective heat transfer is applied to all external boundaries of the TO-220 and heat sink represented by

$$-\mathbf{n} \cdot (-k \nabla T) = h(T_{amb}^4 - T^4) \qquad (2$$

where **n** = unit vector normal to the surface
h = heat transfer coefficient (W/m^2K)
T_{amb} = ambient temperature (K)

A surface-to-ambient radiation is applied to the same set of external boundaries given by

$$-\mathbf{n}\cdot(-k\nabla T) = \epsilon\sigma(T_{amb}^4 - T^4) \qquad (3$$

where ϵ = emissivity

σ = Stefan-Boltzmann constant = 1.38E-23 (J/K)

A constant temperature boundary condition of +10 degrees above ambient is applied to each end of the 3 transistor leads where soldering to the printed circuit board occurs.

5. Model Results

The heat transfer (ht) module is the sole physics interface used since Joule heating in the leads and wire bonds are neglected. The heat transfer in solids sub-interface is attached to all domains. The ambient temperature is consistently set to +20degC (293.15K).

A user-defined mesh calibrated for general physics is set to predefined: normal (maximum 2.9mm, minimum 0.522mm). The maximum element growth rate is left at 1.5, and the resolution of curvature and narrow regions are each 0.5. After meshing, the number of elements is 66,335 with 93,040 degrees of freedom. Figure 3 shows the meshed assembly.

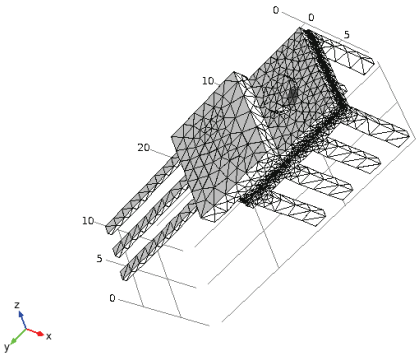

Figure 3. Fully meshed assembly.

The first study is the base case with a power dissipation level of 0.5W and a convection coefficient of 5 W/m^2K (consistent with a low level of natural air flow). Emissivity is set to the values shown previously in Table 2 A stationary 3-D surface plot of temperature is shown in Figure 4 revealing a maximum of +47.3degC or +27.3K above ambient. The heat sink is operating at the high end of the range which should be the case. The PLCC experiences the largest gradient especially along the inner and outer faces. The 3 leads are the coolest point owing the fixed +30degC temperature at the ends.

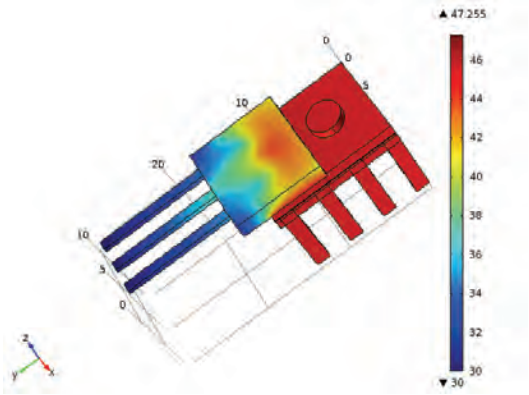

Figure 4. Base case surface temperature.

The temperature profile near the transistor die is illustrated in the slice plot shown in Figure 5.

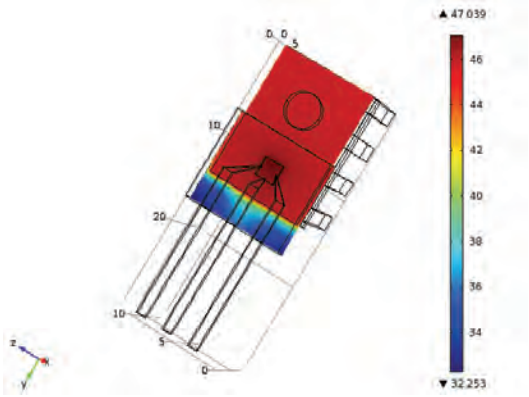

Figure 5. Base case temperature slice.

Slice plots for the base case reveal the maximum temperature at key interfaces of the assembly as

shown in Table 3. Another parameter contained in the table is the temperature above ambient per watt. While an operating temperature of +47degC is not in itself excessive, a rise above ambient of +54degC per watt represents poor heat sinking not surprising considering the low level of air flow and convective cooling (h = 5W/m^2-K).

Table 3. Base case interface temperatures.

Interface	Temperature (degC)	Above Ambient (degC/W)
Transistor die	+47.1	+54.2
Case front	+47.0	+54.0
Case back-mica	+46.4	+52.8
Mica-heat sink front	+45.7	+51.4
Heat sink back	+45.6	+51.2
Heat sink mid-fin	+45.4	+50.8

The next study shows what happens when the overall surface area of the heat sink is increased while leaving the other base case parameters unchanged. Table 4 shows the transistor die temperature as the heat sink area is scaled up 50% in increments of 10%. Based on the results, the relationship between heat sink area and transistor die temperature rise is weak since a 50% area increase only nets a --5.1degC drop.

Table 4. Die temperature versus heat sink area.

Transistor die Relative heat sink area	Temperature (degC)	Above Ambient (degC/W)
Base case	+47.1	+54.2
+10%	+46.6	+53.2
+20%	+46.0	+52.0
+30%	+45.5	+51.0
+40%	+45.1	+50.2
+50%	+44.6	+49.2

The next study examines the impact of surface-to-ambient radiation on the die temperature for the base case. The results reveal a temperature change to +51.7degC, an increase of +3.4degC over the base case where surface radiation is neglected.

The final study focuses on predicting the effect of convection by increasing the heat transfer coefficient, h, from 5 to 50 W/m^2-K in increments of 10. The range for natural convection generally extends from 5 to 25 while above 25, forced convection is required. The results, shown in Table 5, illustrate how important convective cooling is with a temperature reduction from 54.2 to 25.4degC/W.

Table 5. Die temperature versus h.

Transistor die h (W/m^2K)	Temperature (degC)	Above Ambient (degC/W)
5 (Base case)	+47.1	+54.2
15	+41.5	+43.0
25	+38.0	+36.0
35	+35.6	+31.2
45	+33.9	+27.8
55	+32.7	+25.4

6. Thermal Resistance Comparison

The conventional approach to heat sink design uses the concept of thermal resistance. This is a simple method to employ and yields good results.[3-4] This method works as follows. Each transition from one material interface to another is assigned a value expressed as a temperature rise measured in degC/W. The interface resistances are added, and the total is used to compute how much above ambient the die temperature is predicted to be. Computation of the thermal resistance can be complicated depending on the physical geometry, surface-to-ambient radiation, and convective processes involved in the cooling process. Most designers rely on transistor and heat sink manufacturer's datasheets to obtain reasonable values for thermal resistance.

Using the base case results in Table 3, the total and assembly component thermal resistances may be computed. For the die (top row), the above-ambient temperature is +54.2degC/W and represents the total thermal resistance. The difference compared to the case back is +1.4degC/W which represents the die-to-case thermal resistance. From the case back to the mica is also +1.4degC/W. The heat sink

back-to-ambient air is +51.2degC/W for the heat sink. The thermal resistance of the heat sink is of course affected by its physical size/shape, emissivity of the aluminum surface, and the amount of convective cooling present.

While the thermal resistance method is simple, it does not account for some of the nonlinearities in the process. It also does not include the effect of the 3 transistor leads fixed to a printed circuit board where the model assumes a fixed temperature of +30degC. To illustrate, the results of a study to determine how the total thermal resistance varies with power level is shown in Table 6 for a power range of 0.5 to 3W. If the heat conduction process is linear, the total thermal resistance would be constant. Instead, it decreases slightly as the dissipated power increases.

Table 6. Total thermal resistance versus power.

Transistor power (W)	Total thermal resistance (degC/W)
0.5 (Base case)	54.2
1.0	46.9
1.5	44.0
2.0	42.3
2.5	41.1
3.0	40.2

7. Conclusions

This paper discusses the results of several studies that focus on an aluminum heat sink for use with a TO-220 transistor package type. The results show the impact of heat sink area, surface-to-ambient radiation as well as convective cooling. The results are compared to the traditional thermal resistance method of predicting transistor die temperature.

8. References

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