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Investigation of Electromigration in Fine-Pitch Copper Interconnects Through Simulation and Analysis

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Abstract
The scaling down of Copper interconnects is an effective approach to increasing the number of signal I/O lines and performance in advanced fine-pitch packaging for electronic systems. However, as dimensions are reduced, the risk of electromigration-induced failures in the copper interconnects becomes increasingly critical, degrading the reliability and performance of modern microelectronics. High current densities play a crucial role in electromigration, causing the migration of metal atoms in the interconnects, leading to the formation of voids or hillocks and eventual device failure. To reduce the risk of failure and enhance overall performance, Joule heating and current crowding, two significant factors contributing to this problem, must be effectively addressed through design optimization approaches.
Originally, thermal oxide (SiO_2), has been used for dielectric layers. However, the two main challenges for thermal oxide are electrical performance and cost. In such cases, polymer-based dielectrics have advantage due to their ability to lower trace capacitance and enhance power efficiency while being compatible with low-cost panel-scalable methods. But polymers have lower thermal conductivity. By using a thinner polymer, the problem of lower thermal conductivity and consequent Joule heating in the copper interconnects produced by electric current flow across them can be reduced. Therefore, it reduces the risk of localized temperature rise that can cause damage due to thermomigration and electromigration. Current crowding, on the other hand, occurs when there is an increase of the local current density. It raises the local temperature as Joule heating is proportional to the square of current. The conductor's resistance, form, thickness and width have an impact in the current crowding phenomena. This can be managed through optimization of the interconnect geometry, such as having straight lines and using rounded corners. As a result, the potential current crowding hotspots and subsequent electromigration risks can be decreased. COMSOL AC/DC module was used to study the effects of Joule heating and current crowding on interconnect reliability. The simulations included the boundary conditions to corelated experimental values ensuring accurate representation of electromigration. The results thus can be compared to the experimental data to determine accuracy and validity. Through the simulation of current and temperature distribution across the 3D model build in COMSOL, first an improved geometry of the test structure was derived iteratively. The effect of current crowding was reduced with approximately 42% from the standard test layout (STANDARD ASTM-F1259M, US National Institute of Standards and Technology (NIST) test structure) to the optimized structure. Following was a conformation of the effect of polymer thickness.
Therefore, the use of COMSOL simulation provides a powerful means to investigate the effects of different design factors on interconnect reliability. By understanding the comprehensive knowledge gained from these simulations, it is possible to optimize the design and reduce the risk of interconnect failure.
Keywords: Electromigration, Joule heating, current crowding, thermomiogration, fine pitch interconnect reliability, microelectronic system, assembly and interconnection technologies.

Introduction
Finite element analysis (FEA) has become a standard approach for simulating electronic packaging. FEA can be used to predict the warpage of a package, thermo-mechanical reliability of solder joints, reliability of flip chip interconnects under thermal cycling condition, temperature and current distribution in IC devices for certain working condition etc [1][2]. Therefore, FEA is a powerful tool that help in optimizing design, predicting performance, reducing risks and helping with the efficient and reliable product development.
Due to miniaturization of the interconnects in microelectronic systems, electromigration has become one of the dominant failure mechanisms and a major reliability concern. High current densities introduce transport of material, mechanical stress and Joule heating on these fine pitch interconnects. Displacement of metal atoms induces mass depletion or accumulation which subsequently leads to formation of voids and hillocks and causes interconnect failure in form of an open or short circuit [1].
Several methods to alleviate electromigration-induced failure are being developed. Design modification can be done to eliminate the possibility of current crowding on the structure. Influence of various low-k dielectric materials such as polymers to improve the performance of high-density interconnects can be investigated and it can

be an effective approach to reducing the risk of electromigration induced interconnect failure. FEA thus can be used to build up 3D models to analyze multiple design, material choices with their dimensions and simulate at various boundary conditions. This therefore can help in predicting and addressing potential issues, finding optimal solution to enhance reliability and consequently reduce the risks of failure. In this paper we built up a 3D model of a copper interconnect in wafer level along with the adhesive for die attach and substrate. Different design approaches have been considered along with the material choices for the built up. In COMSOL, AC/DC module has been used to simulate the current distribution and Joule heating. The simulations included the boundary conditions to corelated with experimental values. The results thus can be compared to the experimental data to determine accuracy and validity.

Theory

The empirical model to predict the mean time to failure (MTTF) is described by the Black's equation as follows [3][4],

$$\mathrm{MTTF} = A\, J^{-n} \exp\left(\frac{E_a}{k_B T}\right)$$

where A is a cross-section dependent constant, J is the current density, n is the current exponent, E_a is the activation energy, k_B is the Boltzmann constant, and T is the temperature. Thus, Black's equation provides a convenient estimation between the lifetime, current and temperature.

With scaling down of the interconnect, high current density has become a problem. A major concern for the interconnects is the current crowding which is the phenomenon of localized increase of current density in a conductor, typically occurring near contacts or inhomogeneities. This can result in conductor self-heating and accelerated electromigration processes, ultimately leading to failure [5].

The localized high current density can also cause the void growth and at the same time cause the temperature rise due to Joule heating which happens when electric current pass through a conductor. It raises the local temperature as Joule heating is proportional to the square of current. Thermal migration also becomes a concern with Joule heating, as it leads to temperature gradient in the interconnect.

The geometry of the test structure has a significant impact on current crowding. Since the same current is flowing throughout the test structure, due to considerable disparity in the cross-sectional areas between the test line and the contact pads, results in a large and abrupt current density change between the interface of the test line and the pads. As a result, current crowding occurs at the intersections. The higher current density resulting from the current crowding leads to failure at the interface of the test structure due to electromigration. In addition to interfaces, current crowding phenomena are also observed in bends and vias [6].

Dielectrics are the insulators that are used to isolate the copper interconnects. The selection of dielectric material significantly impacts performance such as signaling speed and wiring density. The dielectric constant D_k, an electrical property of the dielectric material, plays a crucial role in determining the signal speed [7].

SiO_2 a dielectric material due to its high D_k value (about 3.8 and thermal conductivity 1.4W/mK) pose challenges to electrical performance as well as cost. In such cases, polymer-based dielectrics have advantage due to their ability to maintain signal integrity and enhance power efficiency while being compatible with low-cost panel-scalable methods [8].

The major limitation with polymer is its low thermal conductivity. Under these circumstances, utilizing a thinner polymer offers a distinct advantage. Thinner layer, acts as a smaller thermal resistor, since conductive thermal resistance $(R_t)_{cond}$,

$$(R_t)_{cond} = \frac{L}{kA},$$

where L is the plane thickness, k is the material conductivity and A is the plane area. So, the heat flow through the layers to the substrate is higher, reducing the Joule heating in the copper interconnect. It also reduces the risk of localized temperature rise that can cause damage due to thermomigration and electromigration.

Furthermore, for fine pitch interconnects planar thin-film polymers are required for impedance matching[8][9].

Governing Equations

The primary focus of our work is to find an optimal process-technically reasonable structure which reduces the effect of current crowding and appropriate polymer thickness that minimizes the Joule heating.

The COMSOL software is utilized to construct a 3D model that incorporates the necessary stack up, consisting of a copper interconnect enclosed within polymer material.

Thermal conduction is the primary mechanism for heat transfer between the copper interconnect and the polymer in this analysis. It is assumed that perfect contact exists between any two surfaces of the materials. The AC/DC module is employed in the multi-physics model, where the electric currents interface is combined with the heat transfer in solids interface through the Electromagnetic Heating Multiphysics interface [10][11] .

Steady state analysis is used to study the steady conduction, the governing equation used in the analysis for heat transfer in a solid is,

$$\rho\, C_p\, (\mathbf{u} \cdot \nabla T) + \nabla \cdot \mathbf{q} = Q \qquad (1)$$

Where ρ is the density, C_p is the specific heat capacity at constant pressure, **u** is the velocity vector and provided the energy equation and responsible for convection in a fluid, T is the absolute temperature, **q** is the heat flux by conduction. The radiation term has been neglected. For a steady-state problem the temperature does not change with time and the terms with time derivatives can be neglected. First and the second term in the left-hand side of the equation (1) represents convection and conduction term of heat transfer. On the right-hand side, the term Q denotes the heat generation or dissipation taking place within the body.
Following Fourier's law of heat conduction, conductive heat flux **q**, is defined by,

$$\mathbf{q} = -k\nabla T \qquad (2)$$

where ∇T is the temperature gradient.
In conductive medium, conservation of electric charges is,

$$\nabla.\mathbf{J} = Q_{j,v} \qquad (3)$$

Where **J** is the current density and, $Q_{j,v}$ is the volumetric source current.
For stationary electric current, Ohm's law state,

$$\mathbf{J} = \sigma\mathbf{E} + \mathbf{J_e} \qquad (4)$$

Where σ is the electrical conductivity, **E** is the electric field strength and $\mathbf{J_e}$ is an externally generated current density, which is suppose to be zero in this study.
Joule's law expresses the Joule heating (ohmic or resistive heating) per unit time as,

$$Q_e = \mathbf{J}.\mathbf{E} \qquad (5)$$

Where Q_e is the heat generated, the **J** and **E** are the current density and electric field strength respectively.
Electric field can also be explained as gradient of electric potential,

$$\mathbf{E} = -\nabla V \qquad (6)$$

Where V is the electric potential.
Coupling between the electric current and heat transfer interface is done through the integration of resistive heating resulting from the electric current into heat generation Q_e (equation (5)).
Thus, putting equation (2), equation (5) in equation (1) we get,

$$\rho C_p\mathbf{u} . \nabla T = \nabla.(k\nabla T) + Q_e \qquad (7)$$

Test structure and Material selection

The test structure use 5µm wide copper interconnect for the simulation. The interconnect is embedded in a polymer which act as a dielectric between the silicon and the interconnect. The 300mm wafer is diced and the die is attached to a KOVAR material using high temperature adhesive (Figure 1a). The copper interconnect is designed for 4-point measurement. The two copper pads are used for current input and ground respectively and the other two copper pads are used for voltage measurement (Figure 1b). The test line attached to the pads carry the current and can be expressed by current density in the line.
To minimize the effect of current crowding, modification in the geometry were made in comparison to standard NIST test structure (Figure 4) [12]. The abrupt change of cross-section was avoided and a more tapered structure was used (Figure 1). A straight test line was chosen over a bent line (Figure 5). These decisions and modifications were carried out by comparing the simulation results, aiming to reduce the impacts of current crowding.
A particular polymer can exhibit a range of viscosity values. Lower viscosity value allows for an application of a thin layer of the polymer through spin coating. Theoretically as mentioned before, a thinner layer should facilitate better heat conduction, thereby reducing the temperature along the test line. Accordingly, we opted for a polymer with a range of viscosity values and corresponding thickness for our test structure in order to examine the correlation between polymer thickness and temperature distribution.
The constructed 3D model (Figure 1c) corresponds to the experimental test vehicle (Figure 2), we therefore attempted to bridge the theoretical concept with simulation and practical application.

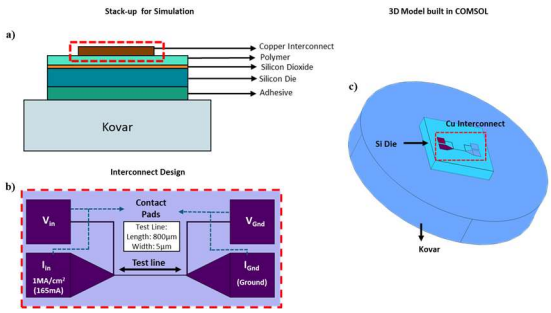

Figure 1: a) Stack-up of the test vehicle, b) The test structure chosen c) COMSOL drawing of the stack-up.

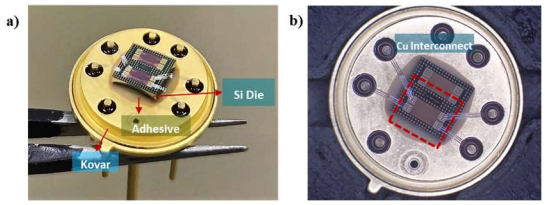

Figure 2: a) Side view of the test vehicle for experiment, b) Top view of the test vehicle.

The material thus chosen for the test vehicle are described in Table 1.

Table 1: Electrical conductivity (σ), thermal conductivity (k) and dielectric constant (D_k) of the material used for the test structure.

Material	σ $(\frac{S}{m})$	k $(\frac{W}{mK})$	D_k	Function
Copper	5.99e7	385	1	Interconnect
Polymer [13]	~ 0	0.29	2.65	Insulator
Thermal SiO_2	~ 0	1.38	3.75	Insulator
Si Die	~ 0	130	11.7	Insulator
Adhesive [14]	~ 0	1.1	5.40	Insulator
KOVAR [15]	2.04e6	17	-	Test Socket

Boundary conditions

Boundary conditions for simulation was chosen such a way that correlation can be done with the experimental values.

To measure current density, biasing has to be done to the pads. In copper the typical current density at which electromigration begins is in the range of 10^6A/cm^2 [16]. Therefore, for the simulation the boundary condition chosen were, corresponding current for 1 x 10^6A/cm^2 current density.

Current density $J = \frac{I}{A}$, where I is the current and A is the cross-section area.

Thus, 165mA is applied to one of the pads and ground on another.

Since the samples are placed in the oven, they will also experience free convection from all the exposed surfaces with surrounding air (oven temperature). Therefore, convective heat flux with heat transfer coefficient (h) of 20W/m^{2}K [16] was applied on all exposed surface.

Table 2: Materials for the test structure and their corresponding dimensions.

Name	L(µm)	w(µm)	h(µm)
Copper interconnect	800	5	3.3
Polymer	3000	3000	1.5
Thermal oxide (SiO_2)			1
Si wafer (diced)			725
Adhesive			50
Kovar	-	-	2000

All the theoretical dimension in Table 2 are close to those from the experiment.

Fine user-control meshing was done to get an accurate result. Mapped and free triangular meshing was used for the interconnect with element size of minimum 2µm to maximum 10µm depending upon the structure. The die and the rest of the structure was meshed with free quad with element size of 70µm. Followed by sweep with fixed number of elements in distribution being 4.

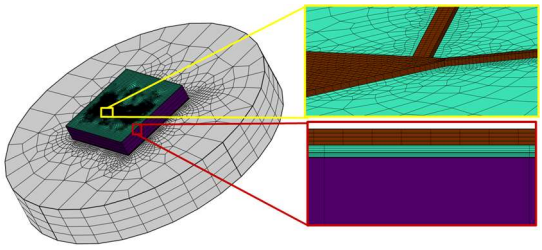

Figure 3: Meshing of the 3D test structure.

Discussion

Initially, we conducted a comparison between the NIST structure for electromigration testing [12] and our proposed structure, concerning current crowding effects.

Current density we used for all the simulations were 1 x 10^6A/cm^2.

In the NIST structure Figure 4a, we identified two significant areas of concern related to current crowding, primarily caused by the abrupt change in cross-sectional area. As a result, by modifying the geometry as shown in Figure 4b, the current crowding decreased by approximately 42%.

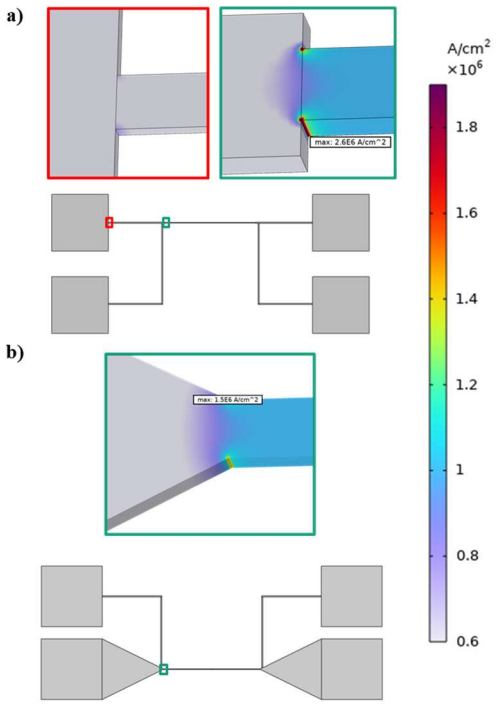

Figure 4: Comparison of a) NIST with b) Optimised design on current crowding.

We additionally conducted simulations with a 90° bent test line to validate the theory of current crowding in the inner edge of the turn. We explored potential solutions to alleviate current crowding by rounding the corners. We also investigated the impact of the arc radius of the rounded corner on current crowding (Figure 5).

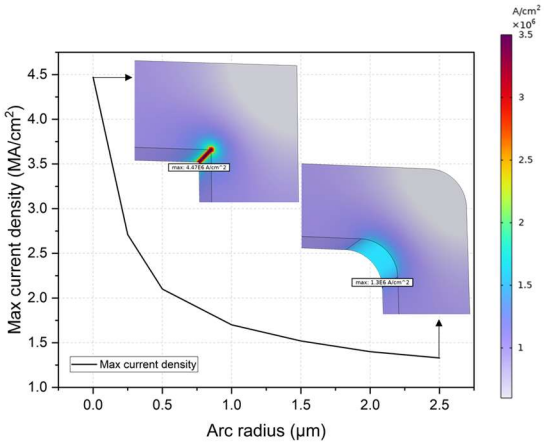

Figure 5: Influence of arc radius in the 90° angled line, on current density.

To decrease the current crowding at the junction of the pads and the test line in the optimized design, we adhered to the aforementioned principle by rounding off the corners to reduce sharp edges. By increasing the arc radius, the initial current was reduced by approximately 33%.

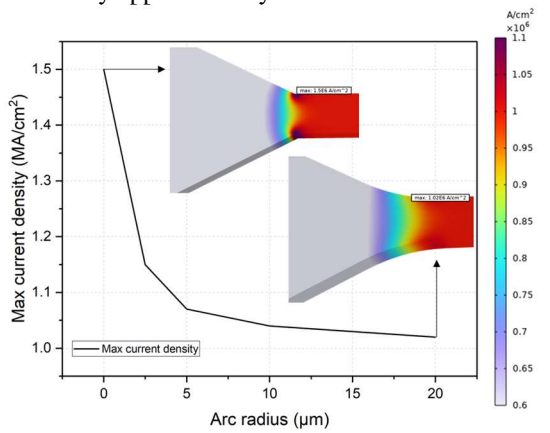

Figure 6: Influence of arc radius in the transition area on current density.

We also used simulation to confirm the initial theoretical premise that thinner polymers exhibit better heat conduction characteristics (Figure 7). With simulation result conforming the theoretical concept, we build up a test chip (Figure 2) with optimized geometry and thinner polymer layer (1.5μm). Experiment on the test chip specifically the Temperature Coefficient of Resistance (TCR) test was conducted. The purpose was to verify the correlation between the simulation results and the experimental observations. Temperature coefficient of resistance (TCR) is the calculation of a relative change of resistance per degree of temperature change. Positive coefficient value for a material means that its resistance increases with increase in temperature.

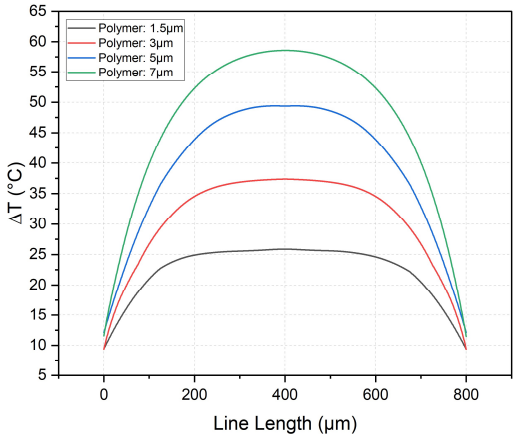

Figure 7: Influence of polymer thickness in temperature distribution.

Joule heating experimentally can be found out by the TCR test. By applying varying currents at a constant temperature, changes in resistance can be observed. The increase in resistance compared to an initial resistance is a result of Joule heating. Furthermore, the magnitude of the temperature rise can be calculated based on the formula below.

$$R = R_0[1+ \alpha(T-T_0)]$$

Where, R is resistance at temperature T, R_0 is the initial resistance of the test structure at T_0, α is the co-efficient of resistance, T is the temperature of the test structure and T_0 is the initial temperature. The value of α was determined experimentally and subsequently utilized in the equation to calculate the temperature.
We performed an experiment using first samples to investigate Joule heating, ΔT which is $T-T_0$. The average of the obtained results was 28±1°C.
The ΔT value obtained from the COMSOL simulation (polymer 1.5μm) was 25°C (Figure 7), a result that closely aligns with the experimental measurement.
The small difference between the values observed in reality and those obtained through simulation primarily arise from two key factors. Firstly, simulations assume a perfect structural configuration and secondly, it uses standard material properties. Whereas, actual fabricated structures often deviate from ideal dimensions and material characteristics.

Conclusions

This study demonstrates the application of finite element modeling for assessing the electromigration reliability of fine-pitch copper interconnects. Using AC/DC module of COMSOL and Electromagnetic Heating Multiphysics, it effectively simulates and observes critical issues such as Joule heating and current crowding in the interconnects. These simulation results thus can be used to further optimize the design to reduce Joule heating and current crowding, consequently reducing the risk of electromigration failure. The

boundary conditions used in the simulation are consistent with experimental value, aligning the experiment's outcomes with those from COMSOL. Therefore, finite element modeling offers semiconductor manufacturers valuable insights, allowing them to explore different designs and optimization possibilities tailored to their requirements while minimizing time and cost. Future work will focus on the effect of Blech's length on electromigration immortality and material flux density on interconnect reliability.

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